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COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECOENGINEERING RELEASE	10/16/2018	R. PERRY

A

B

C

D

E

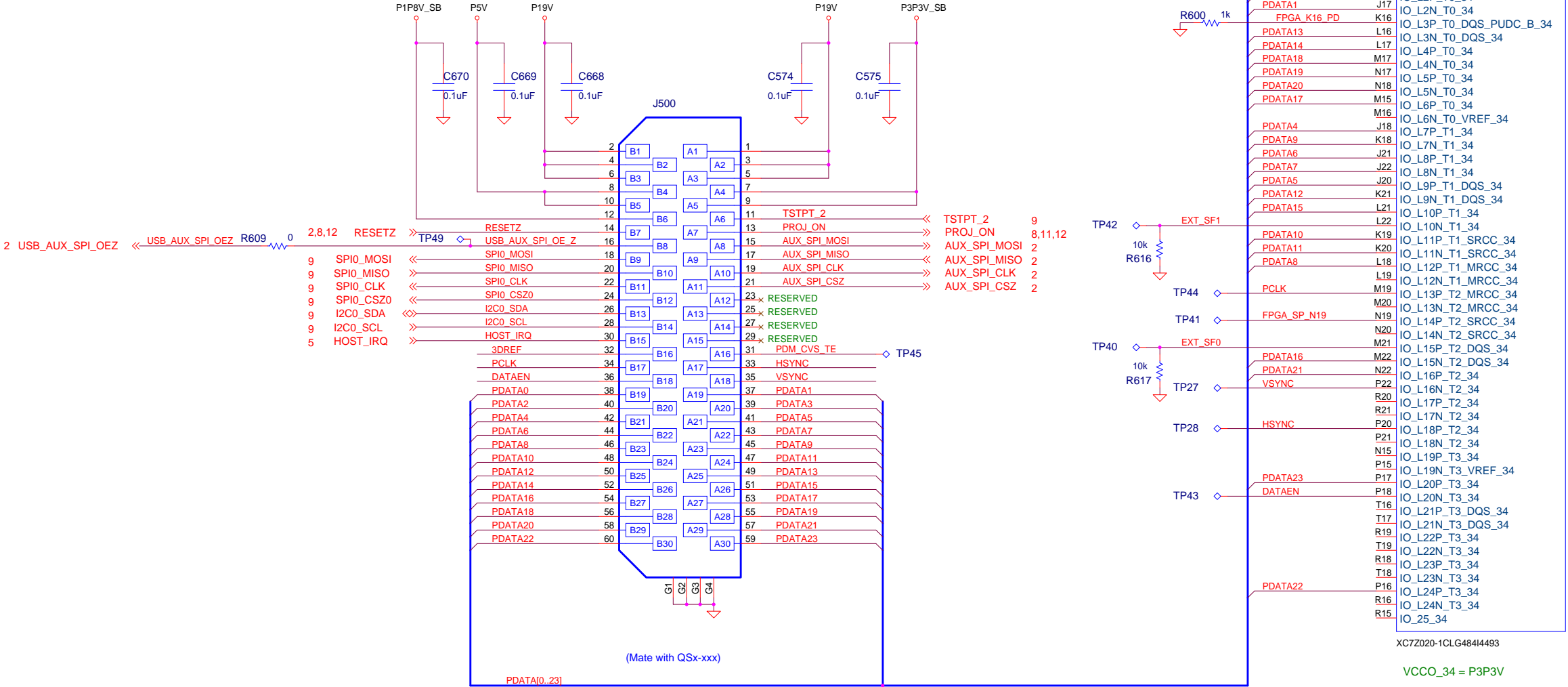
F

DLPC3436 1080p DISPLAY BOARD
REFERENCE DESIGN

DWN	Roger Perry	DATE	OCT-16-2018	TEXAS INSTRUMENTS - DLP® Products		
ENGR	Roger Perry	OCT-16-2018		(C) COPYRIGHT 2018 Texas Instruments Inc. All Rights Reserved		
SYS	Paul Rancuret	OCT-16-2018		TITLE DLPC3436 1080p Display Board		
APVD	Jeff Dennis	OCT-16-2018		DRAWING NO 2516437		REV A
QA				11 x 17	Orcad Capture 16.6	SHEET 1 of 16

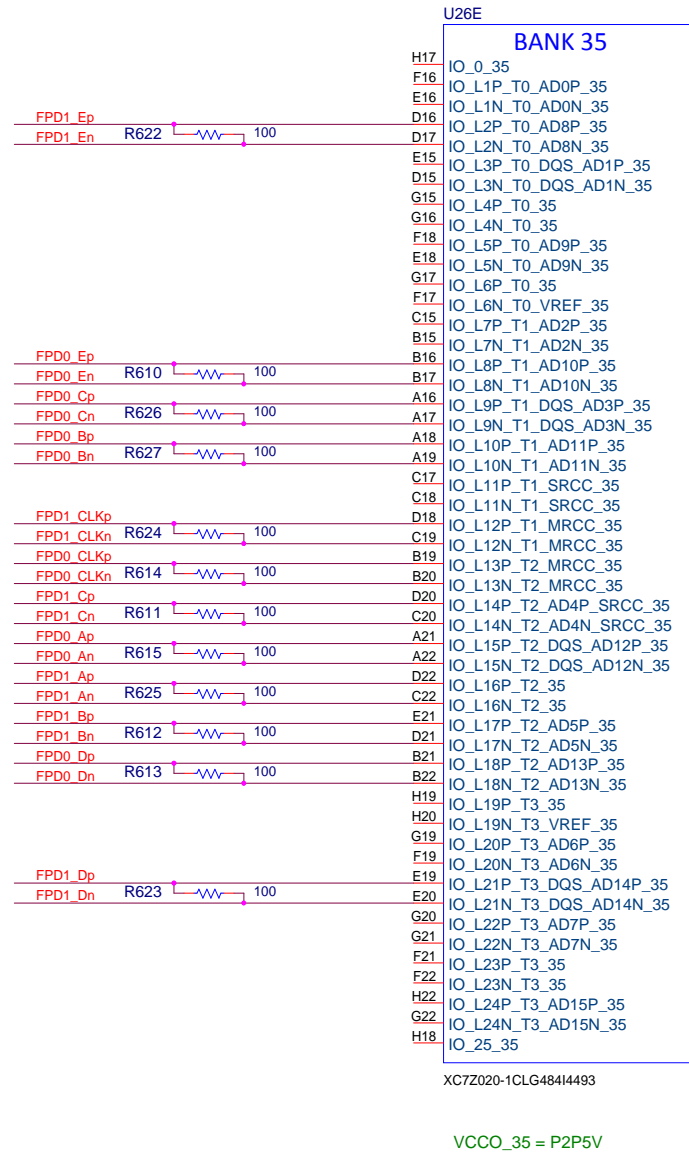
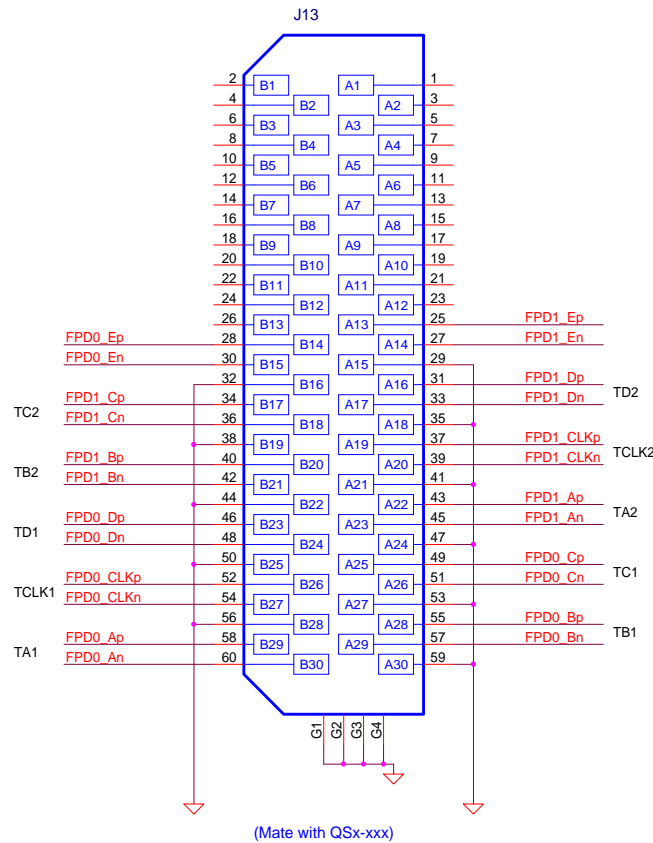
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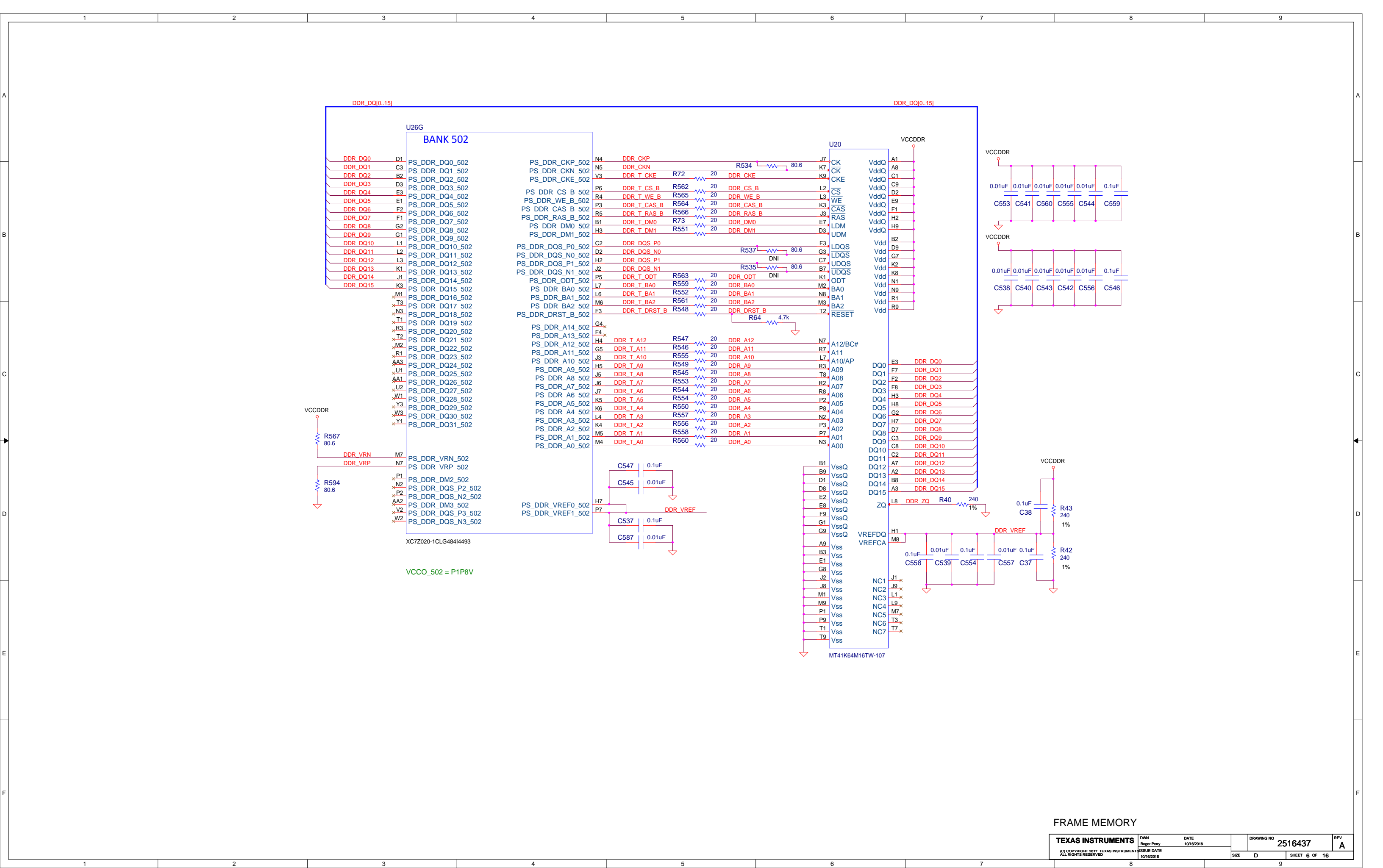
CONNECTION TO FRONT END PROVIDING PARALLEL RGB VIDEO INPUT
(PLACE ON BOTTOM SIDE)



FPGA Parallel Data Input Interface

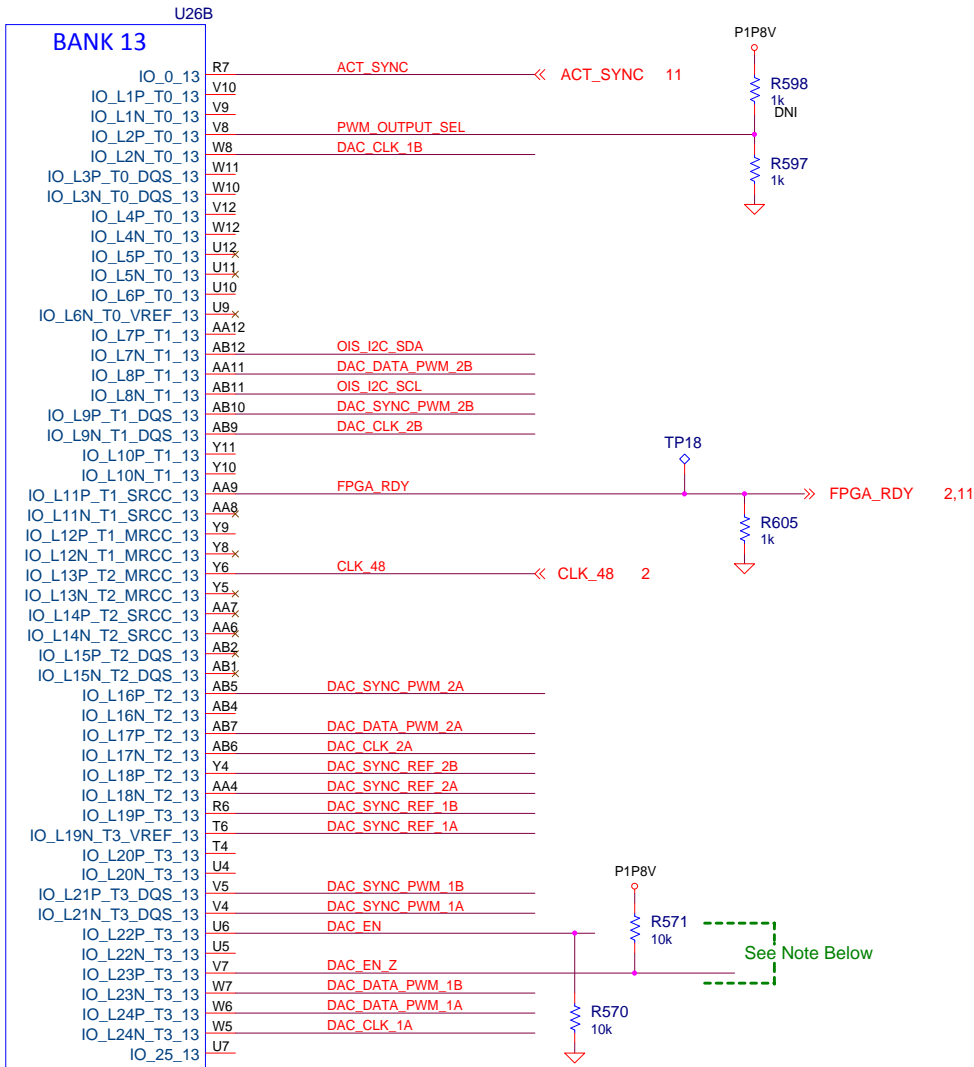
CONNECTION TO FPD LINK VIDEO INPUT
(PLACE ON TOP SIDE)





FRAME MEMORY

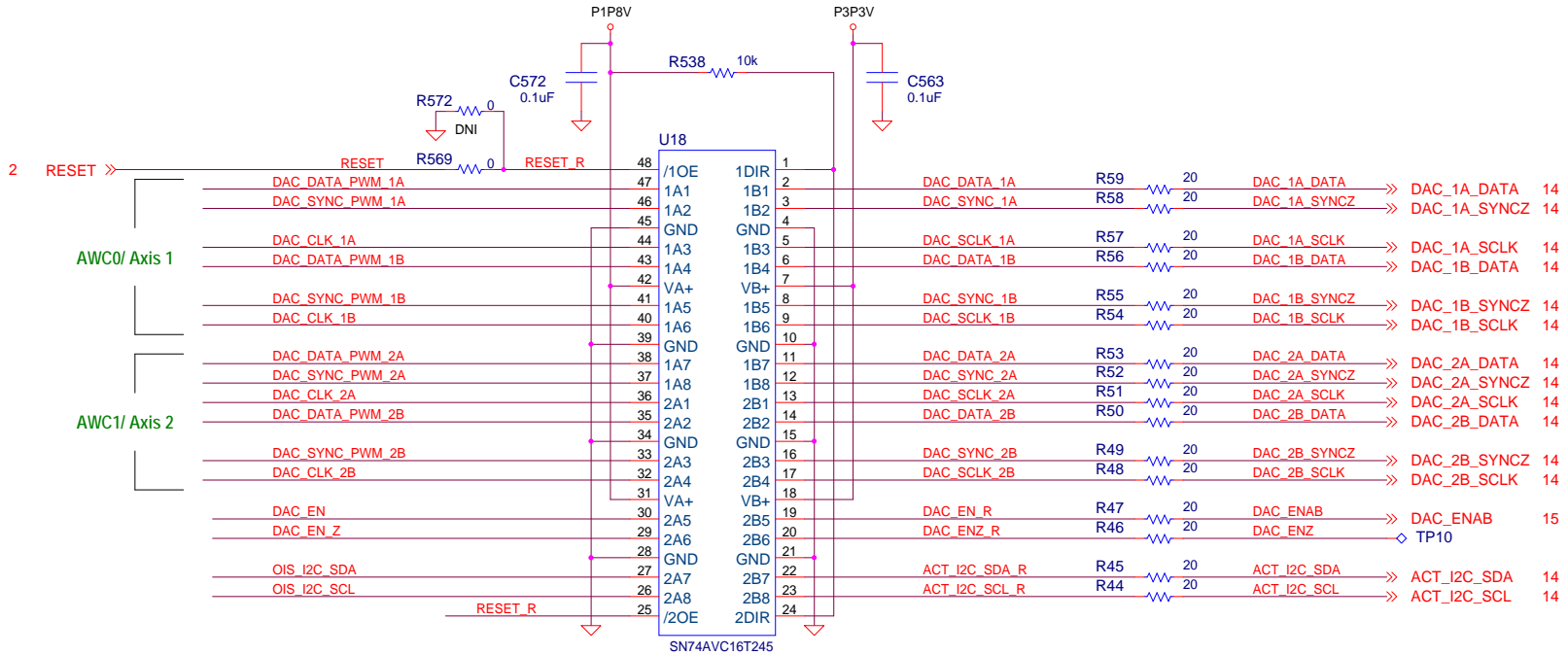
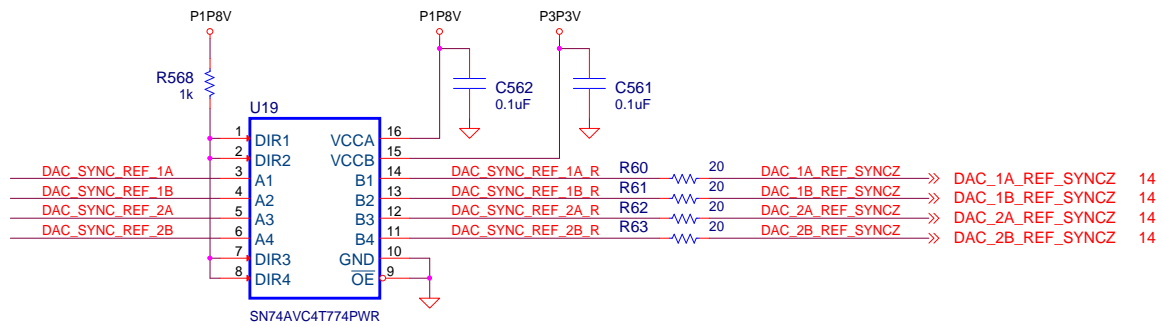
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	ISSUE DATE 10/16/2018	SIZE D	SHEET 6 OF 16	



XC7Z020-1CLG484I4493

VCCO_13 = P1P8V

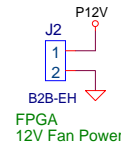
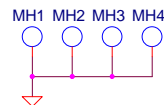
NOTE:
It is recommended to only use the DAC_EN signal to control the power up of the actuator drive circuit if needed.
The DAC_ENZ signal can not be pulled-up in the case no power is applied to the FPGA. Therefore the use of the DAC_ENZ signal is not recommended. If the DAC_ENZ needs to be used additional logic must be implemented to avoid an uncertain state of the DAC_ENZ signal during power-up.



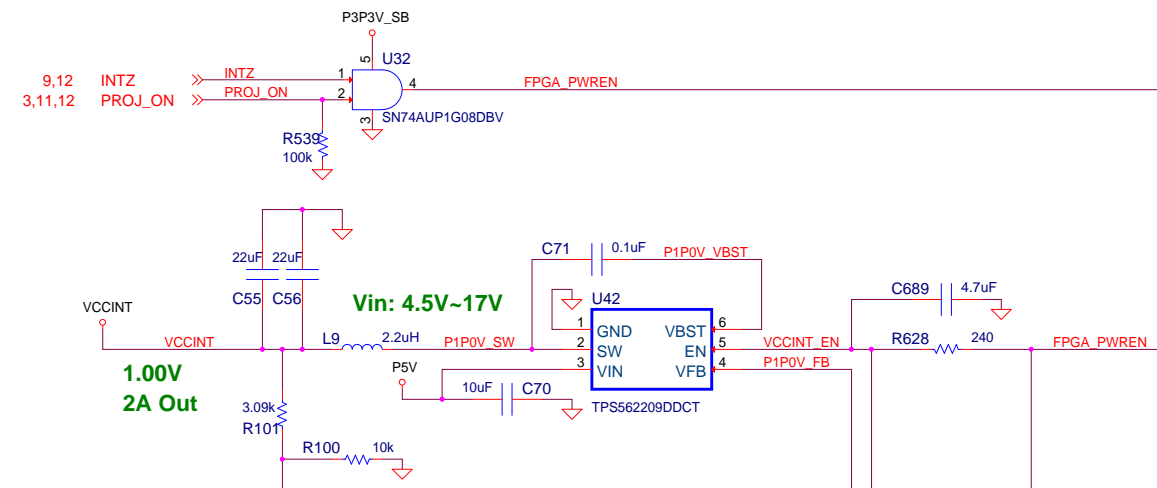
DAC INTERFACE

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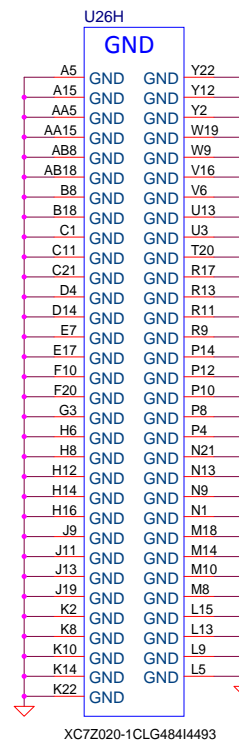
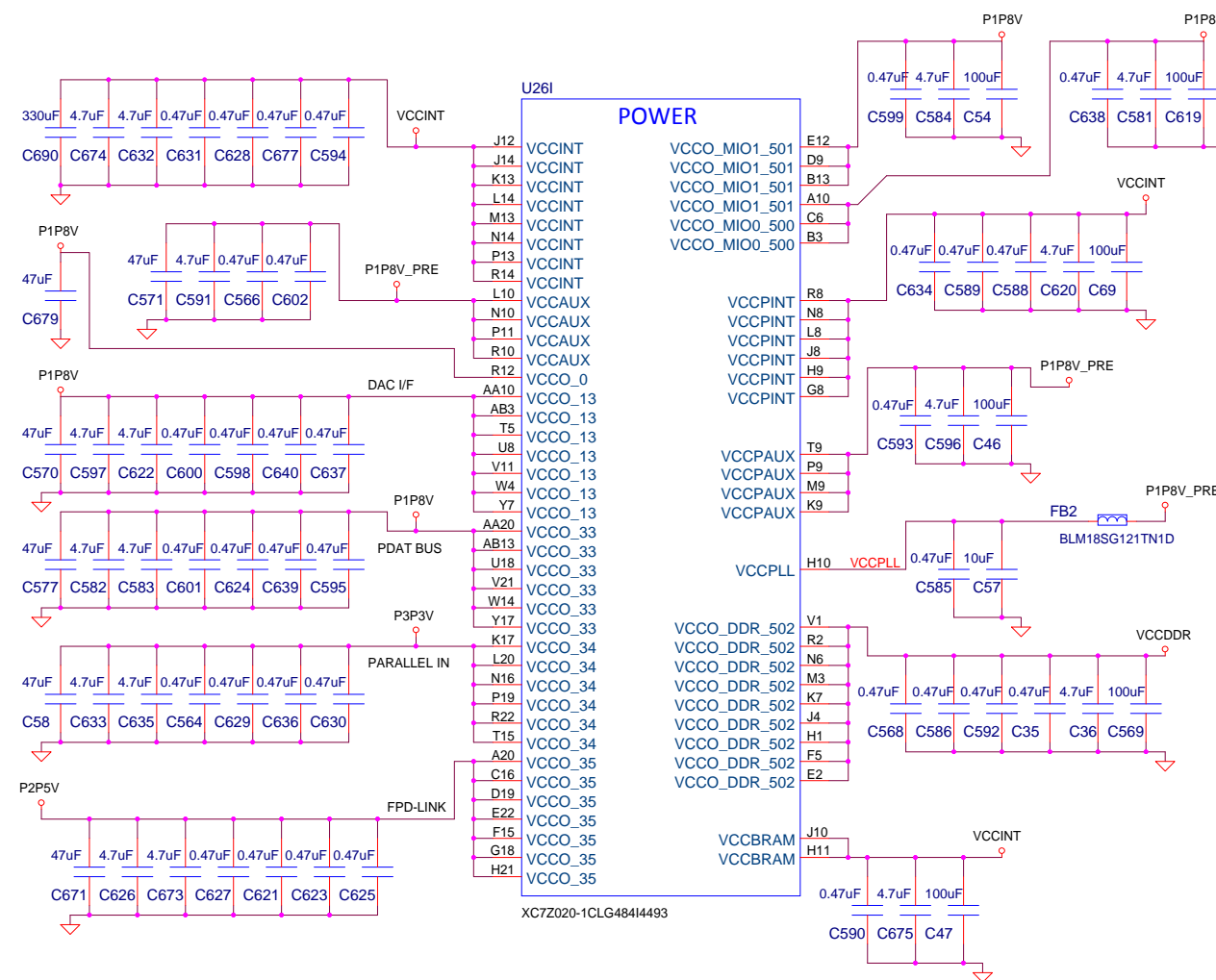
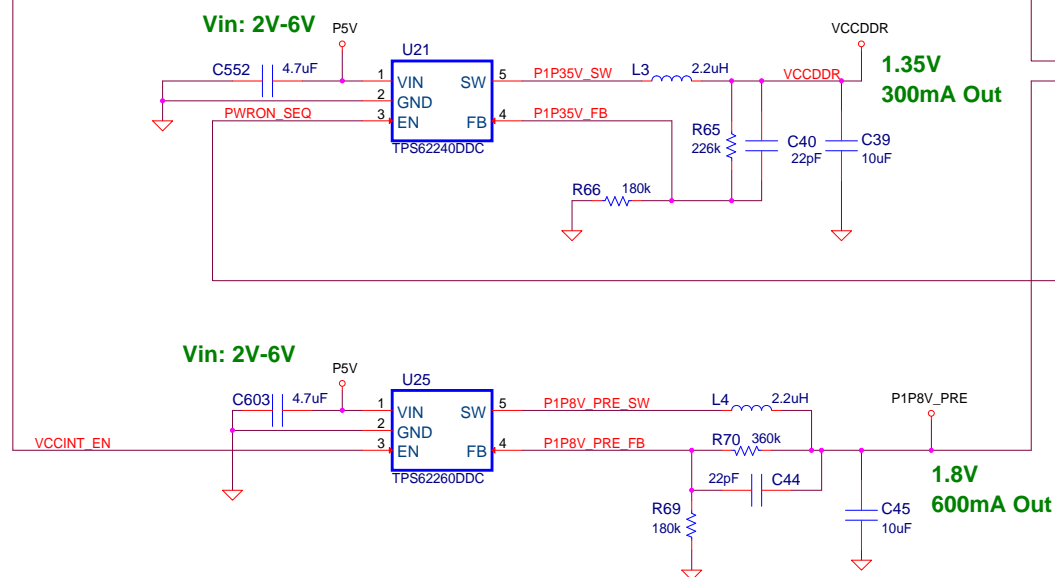
BOARD MOUNTING HOLES



- SHUTDOWN WHEN FAST PARK DETECTED.
- INTZ GOING HIGH ENABLES POWER TO FPGA.

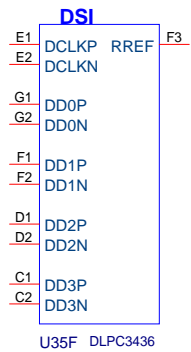
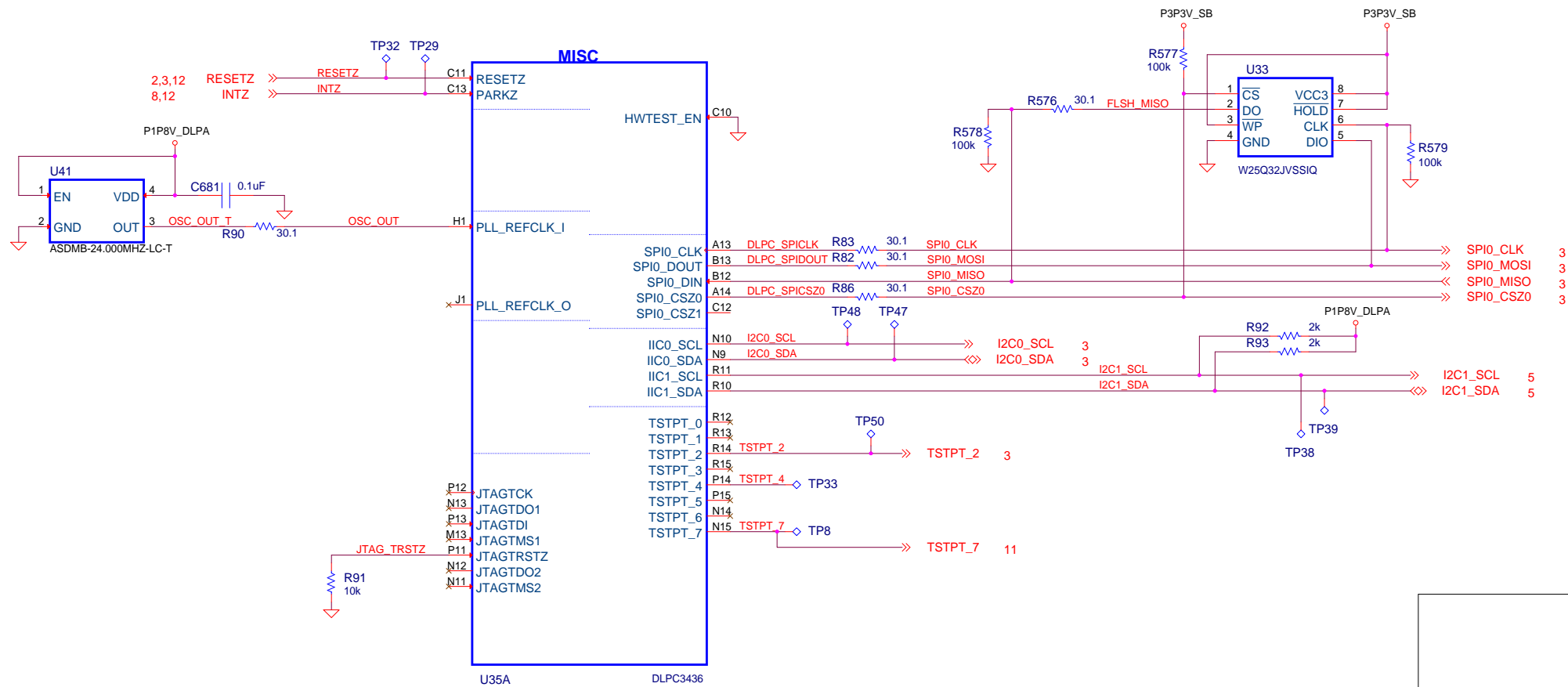


LOAD SWITCHES FOR I/O POWER



FPGA POWER

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The DSI Port is not supported by the DLPC3436. Inputs are left unconnected per datasheet recommendation.

DLPC3436 ASIC, Clock,
SPI Flash Memory & DSI

DMD INTERFACE

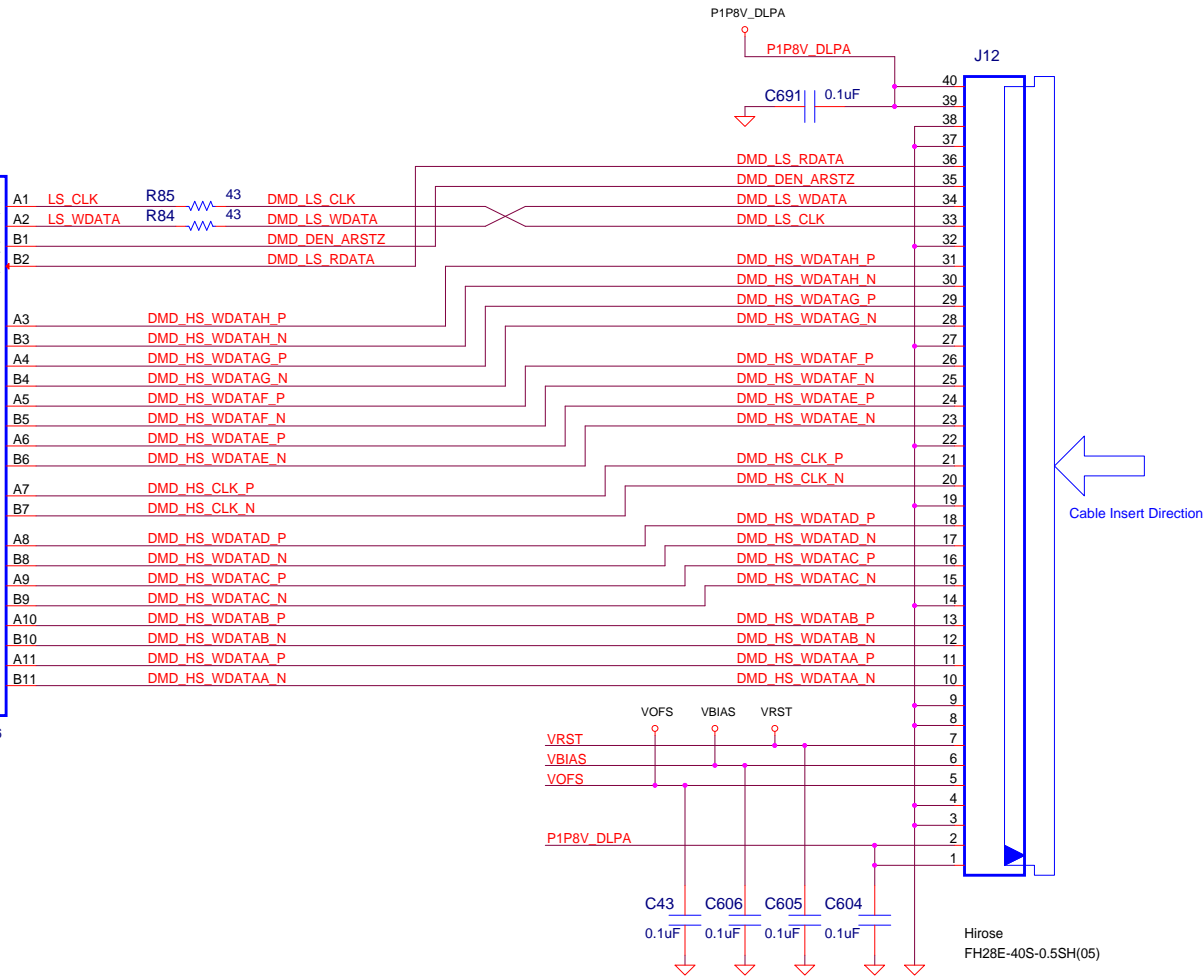
DMD_LS_CLK
DMD_LS_WDATA
DMD_DEN_ARSTZ
DMD_LS_RDATA

DMD_HS_WDATAH_P
DMD_HS_WDATAH_N
DMD_HS_WDATAG_P
DMD_HS_WDATAG_N
DMD_HS_WDATAF_P
DMD_HS_WDATAF_N
DMD_HS_WDATAE_P
DMD_HS_WDATAE_N

DMD_HS_CLK_P
DMD_HS_CLK_N

DMD_HS_WDATAD_P
DMD_HS_WDATAD_N
DMD_HS_WDATAC_P
DMD_HS_WDATAC_N
DMD_HS_WDATAB_P
DMD_HS_WDATAB_N
DMD_HS_WDATAA_P
DMD_HS_WDATAA_N

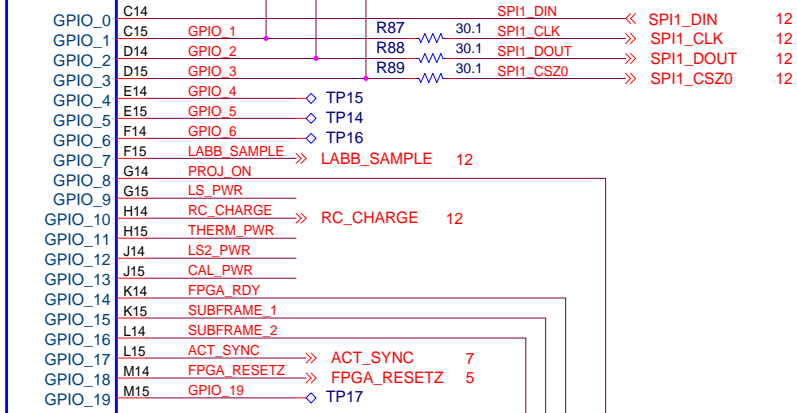
U35B DLPC3436



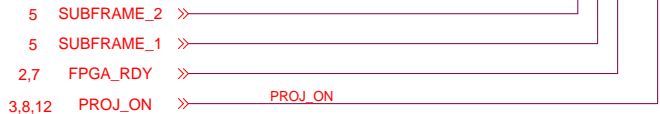
- DMD_LS_RDATA ◇ TP_RD
- DMD_DEN_ARSTZ ◇ TP_ARZ
- DMD_LS_WDATA ◇ TP_WD
- DMD_LS_CLK ◇ TP_CLK
- DMD_HS_CLK_P ◇ TP_CKP
- DMD_HS_CLK_N ◇ TP_CKN
- DMD_HS_WDATAA_P ◇ TP_AP
- DMD_HS_WDATAA_N ◇ TP_AN

DMD INTERFACE

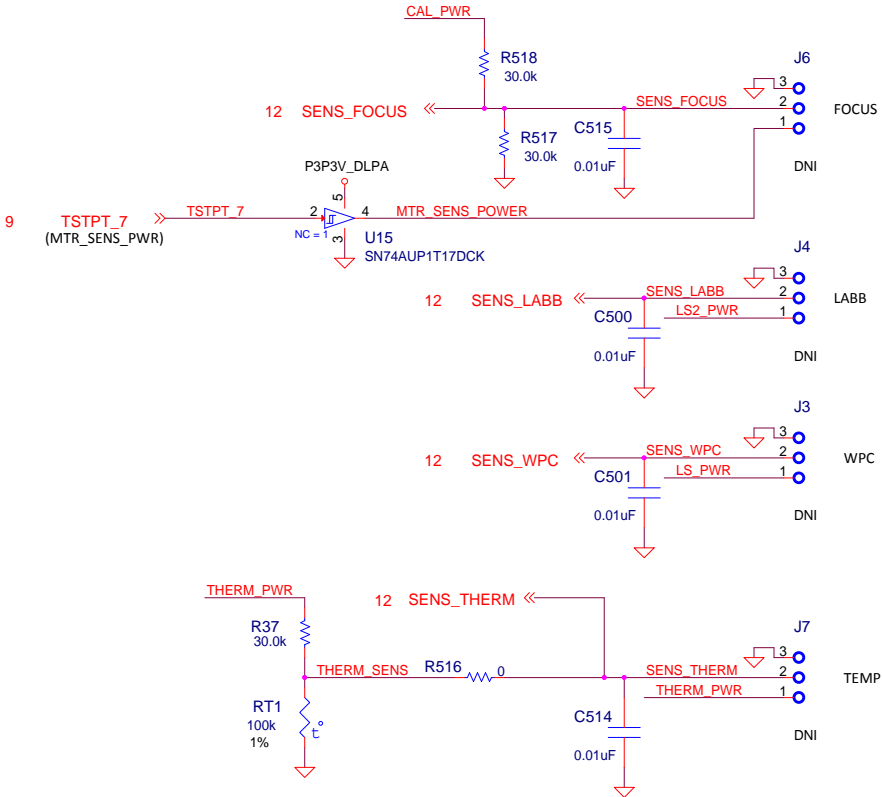
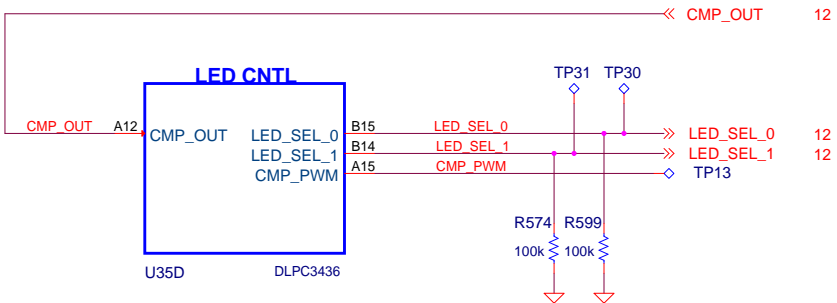
GPIO



U35C DLPC3436



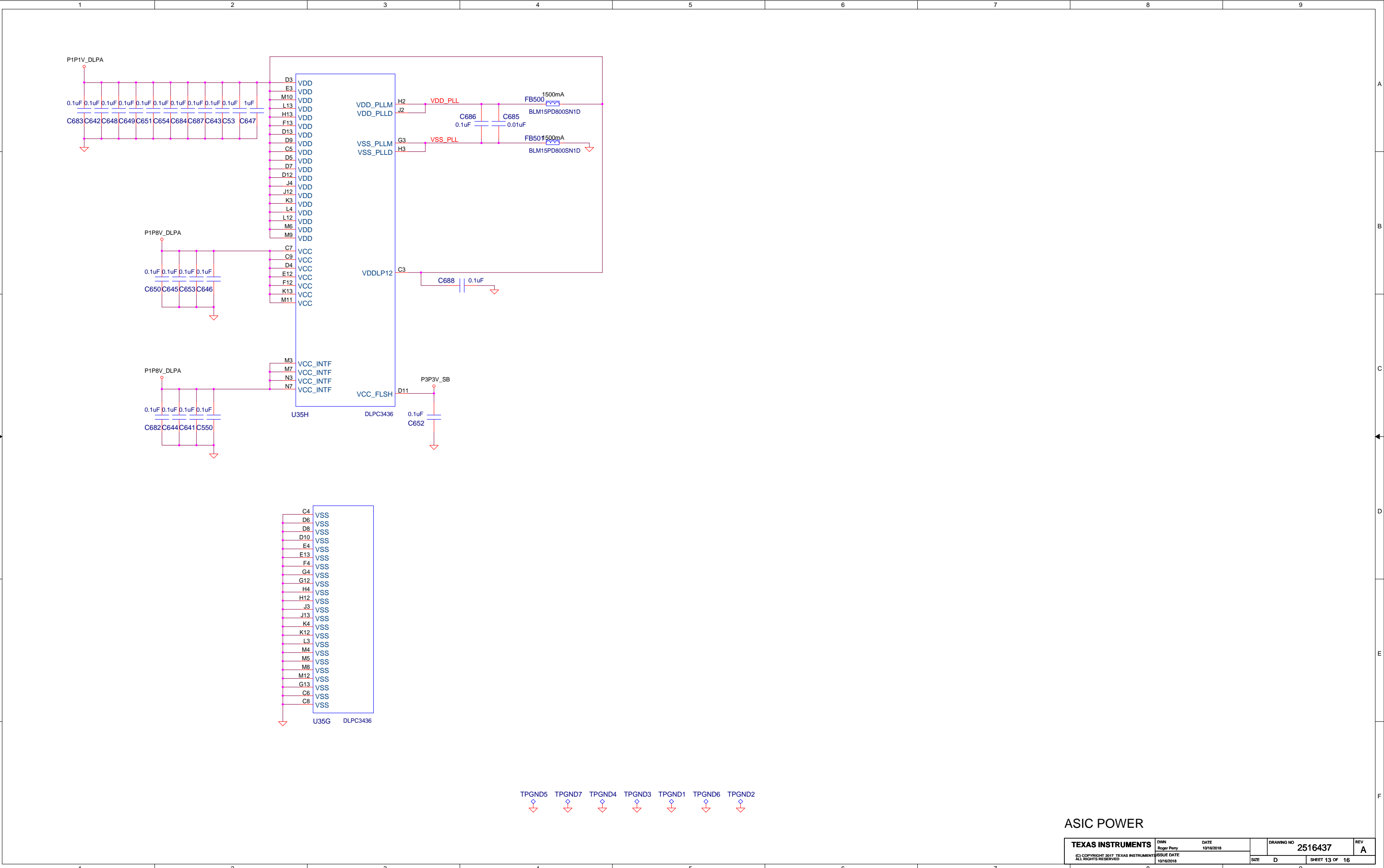
LED CNTL



DLPC3436 GPIO, SPI1 BUS & LED_SEL

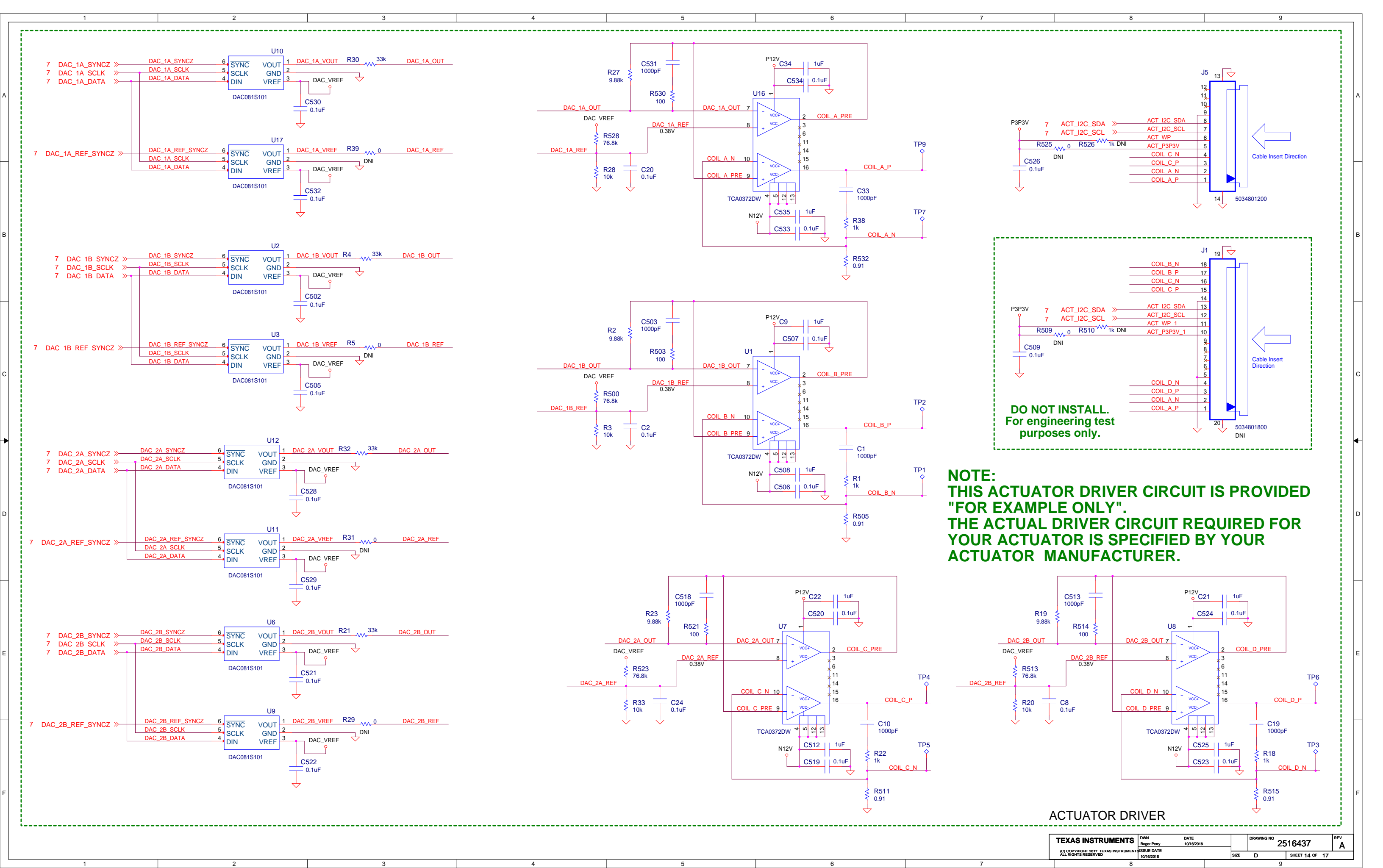
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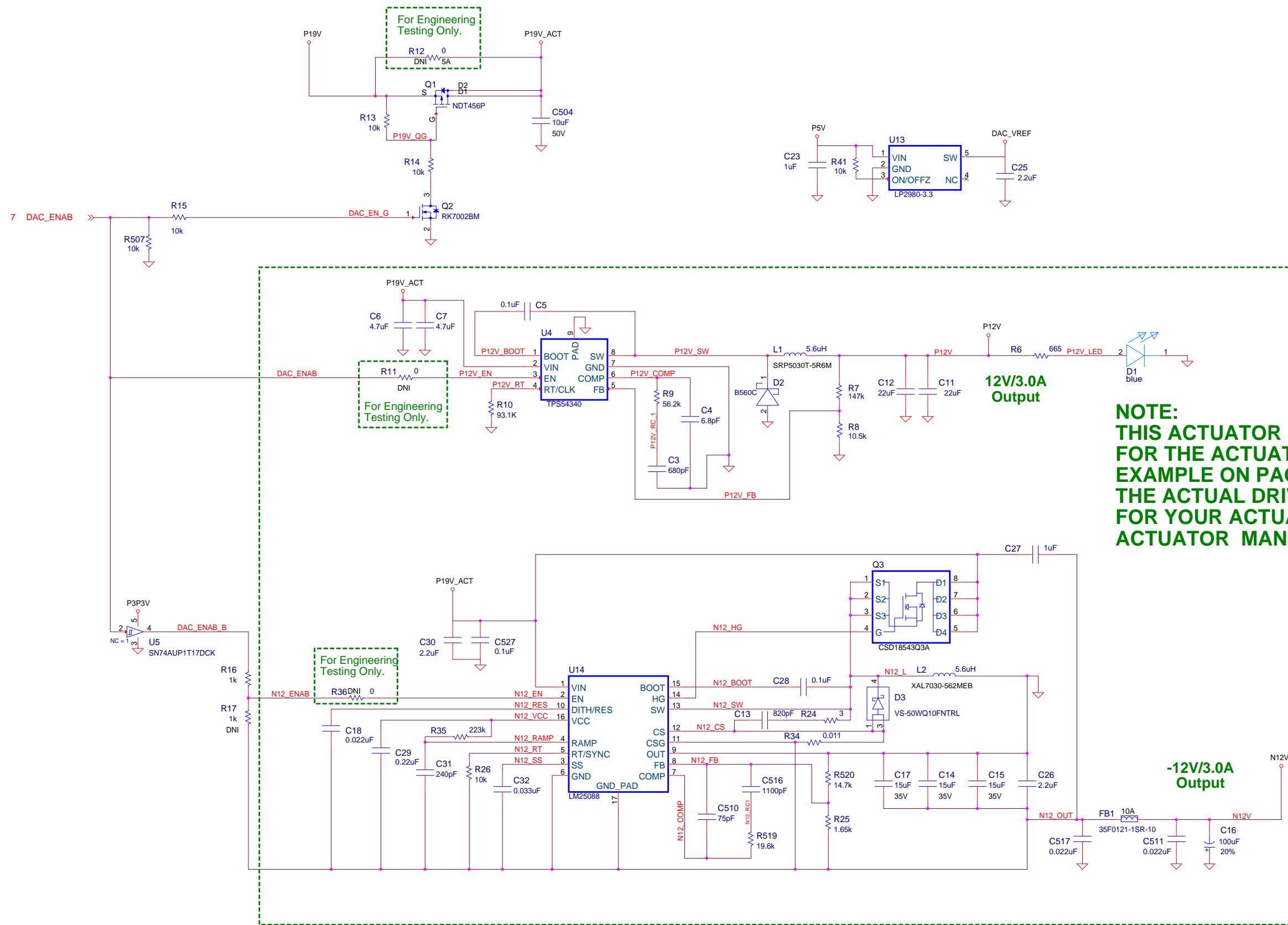




ASIC POWER

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	ISSUE DATE 10/16/2018			





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A	<div>Revisions</div> <div>Rev. A: Initial Release</div>								A
B									B
C									C
D									D
E									E
F									F
1	2	3	4	5	6	7	8	9	

REVISION NOTES

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1	2	3	4	5	6	7	8	9	
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B									B
C									C
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